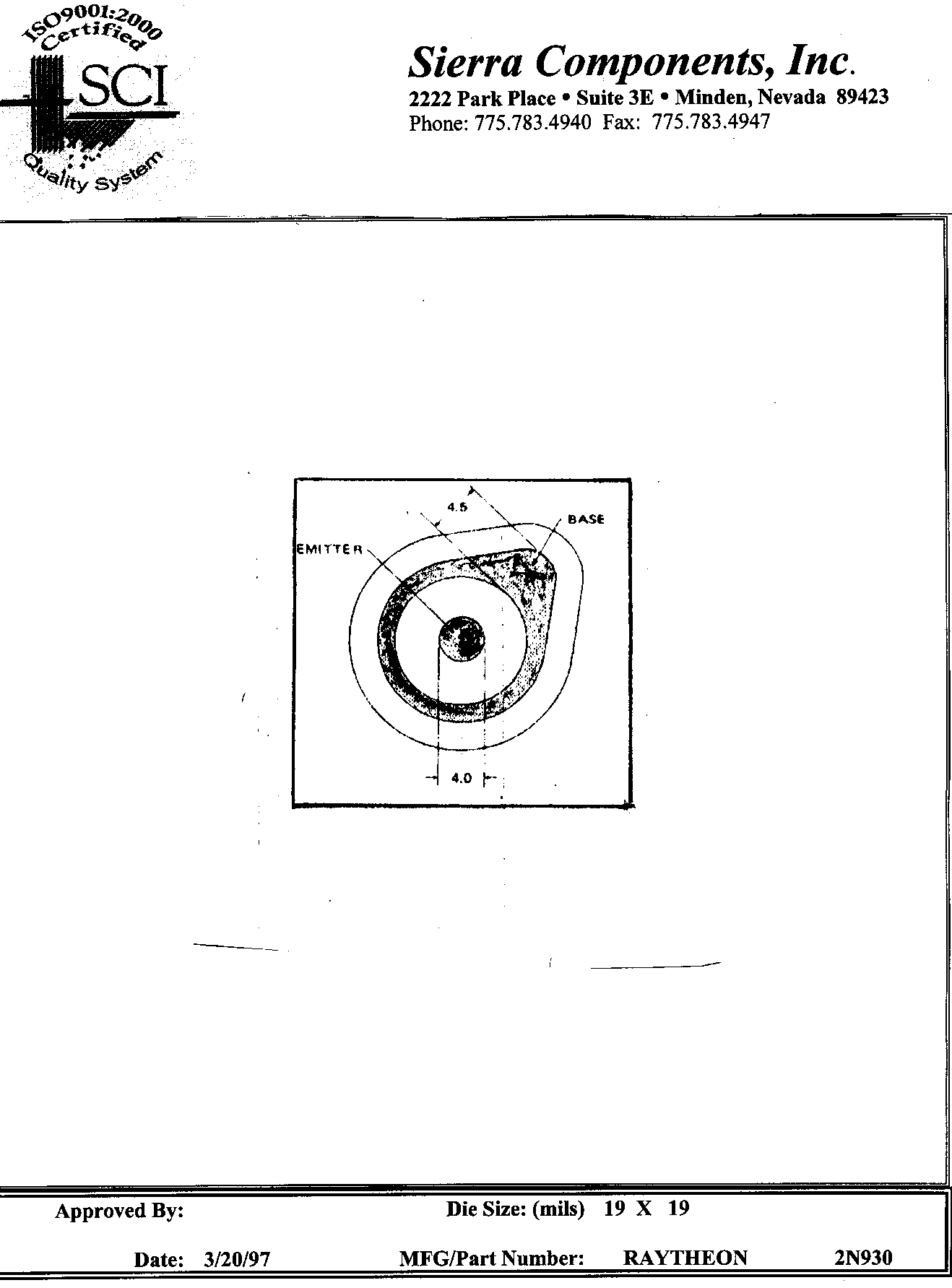
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.019”**



**.019”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .019” X .019” DATE: 11/15/21**

**MFG: RAYTHEON THICKNESS .000” P/N: 2N930**

**DG 10.1.2**

#### Rev B, 7/1